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(54) Abstract Title
Multi-layer circuit board with layers acting as a "heat capacitor"

(57) A circuit board (1) includes at least one substrate (2) having a first layer (5) and at least one second layer (6), wherein the first layer (5) and at least the second layer 6 are used for heating a component (22) to be soldered to at least one of the layers (5,6), the layers acting as a "heat capacitor" when the circuit board is placed in a reflow oven or the like. This allows the soldering of components which require a larger amount of heat at the same time as other components. The part of the circuit board containing the "heat capacitor" layers may be separated from the rest of the board after soldering, e.g. by means of a frangible connection (32, see Fig. 1).

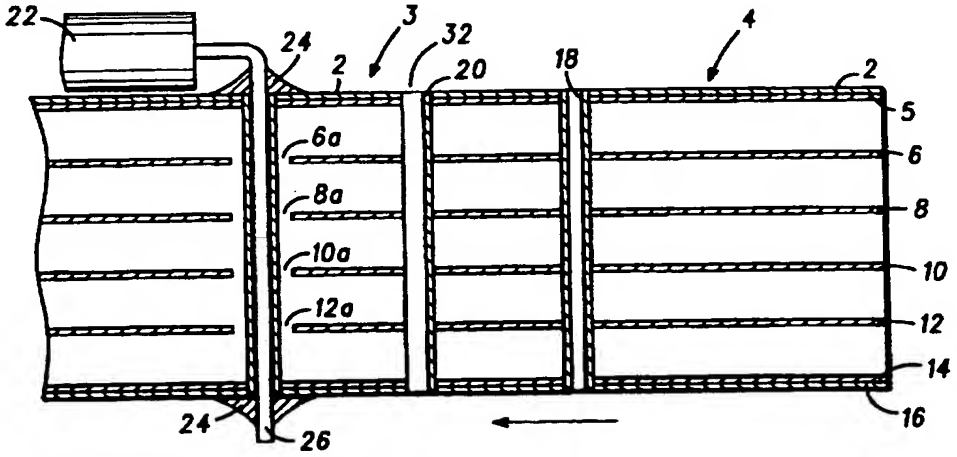

FIG. 2

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At least one drawing originally filed was informal and the print reproduced here is taken from a later filed formal copy.

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CIRCUIT BOARD

Field of the Invention

This invention relates to a circuit board. The invention is particularly applicable to, but not limited to, soldering a device to a printed circuit board with the use of a reflow process.

Background of the Invention

There are several methods and process to solder components to a circuit board and especially to a Printed Circuit Board (PCB). The methods will now be briefly described.

The first method is a method of soldering a component to the PCB by a solder iron. The soldering operation will be done by a human. The method includes the steps of: applying a soldering compound to legs of the component and melting the soldering compound on the component legs using the soldering iron to join the legs to conductive tracks of the PCB.

The second method is a wave soldering process. The method includes the steps of: inserting the components to the PCB and passing the PCB bottom substrate over a bath which contains a molten solder compound.

The third method is that of soldering the components to a PCB in a reflow oven. This method is particularly applicable to a legless surface mount components and is known in the art as a reflow soldering process. The reflow soldering process consists of applying solder paste on at least one side of the PCB, placement of the components on the solder paste and soldering of the components in the reflow oven (the heat of the oven rendering the compound molten). When a large mass component is applied to the PCB, a large amount of heat is required to solder, and a two stage soldering process is needed. The first stage is a reflow process and the second stage is a wave soldering process or manual soldering of the large mass component.

The disadvantage of soldering components with a use of at least two methods of soldering is that, the soldering process includes two stages expanding the manufacturing process for the PCB. The soldering process also needs at least two types of soldering devices that is to say a soldering iron and a reflow oven or solder bath.

This invention seeks to provide a PCB which mitigate at least some of the above mentioned disadvantages.

Summary of the Invention

According to the invention there is provided an circuit board. The circuit board includes at least one substrate having a first layer and at least a second layer wherein the first layer and at least the second layer are in use for heating a component to be soldered to at least one of the layers. The circuit board includes a first portion and a second portion. The second portion is in use used as a heat capacitor. The heat from the second portion is transferred to the first portion to solder the component which needs an higher temperature then the other components which are placed on the first portion.

Advantageously, by the use of the present invention only one pass and one soldering device are use in the soldering process of the circuit board.

In the preferred embodiment, of the invention the substrate has at least two portions and which the second portion extending beyond the periphery of the board and being frangibly connected to the first portion.

Preferably, there are provide a plurality of second layers.

In this manner, at least one of the second layers is or are formed within the board.

In the preferred embodiment of the invention, the layers of the first portion are connected to the layers of the second portion which the first layer and at least one of the second layer are connected to each other.

In this manner, the second portion is in use used as heat capacitor for accumulating heat provided by a soldering device.

Preferably, the soldering device is a reflow oven.

In the preferred embodiment, the heat transfers from the second portion to the first portion through a frangible connection.

In the preferred embodiment, breaking of the frangible connection between the first portion to the second portion will cause disconnection of the layers.

Preferably, the first layer and at least one second layer are made of Copper.

A preferred embodiment of the invention will now be described by way of example only, with reference to the drawing.

Brief Description of the Drawings

FIG. 1 is a circuit board according to a preferred embodiment of the invention;

FIG. 2 is a cross section A - A of the circuit board of FIG. 1; and

FIG. 3 is a cross section B - B of the circuit board of FIG. 1.

Detailed Description of the Drawings

Referring firstly to FIG. 1, a circuit board according to a preferred embodiment of the invention is shown. The circuit board 1 includes a top substrate 2 having two portions, a first portion 3 and a second portion 4. The second portion 4 extends beyond the periphery of the circuit board 1 and is frangibly connected to the first portion 3. The second portion 4 is in the soldering process used as a heat capacitor for accumulating heat which is provided by a soldering device, for example a reflow oven (not shown).

In operation, the reflow oven applies heat to the circuit board 1. The heat is accumulated in the second portion 4. The heat is transferred from the second portion 4 to the first portion 3 by layers of the circuit board 1 layers. A detailed description of the operation will be described with reference to FIG. 2 and FIG. 3.

Referring now to FIG. 2, a cross section along line A - A of Detail A of FIG. 1 is shown. The circuit board 1 includes a top substrate 2, having a

first layer 5, a second layer 6, a third layer 8, a fourth layer 10, a fifth layer 12, a sixth layer 14 and a bottom substrate 16. The layers 5, 6, 8, 10, 12, 14 and the substrates 2 and 16 of the second portion 4 are connected by a through hole plate via 18 and an edge plating 20 of copper to form a heat capacitor. The layers 5, 6, 8, 10, 12, 14 are formed within the board during manufacture by a plating technique as the board layers are built up. It will be seen that the layers are provided with non-plated regions, for example, 6a, 8a, 10a and 12a. At these regions component retaining holes will be provided in a drilling operation. It is necessary to provide the non-plated regions to ensure that the component leg is not connected by means of the layers to other components. The first layer 5 and the layers 5, 6, 8, 10, 12, 14 are made of copper and the compound between the layers is made from glass reinforced resin (glass-epoxy). The second portion 4 is used for heating a component 22 to be soldered to at least one of the layers. The following equation will show the heat capacitance which is needed to solder the component 22 to at least one of the layers.

$$C_{TH} = MC_p = \sum_{i=1}^{x} A_G \bullet t_G \bullet \rho_G \bullet C_{Pa} + \sum_{i=1}^{x} A_{Cu} \bullet t_{Cu} \bullet \rho_{Cu} \bullet C_{Cu}$$

wherein

C_{TH} - is the heat capacitance needed to solder a component

M - is the mass of the component,

C_p - is thermal coefficient of the material of the component,

A_G - is the area of the circuit board

(G - is for Glass-Epoxy, Cu - Copper),

t_G - is the thickness of the circuit board,

ρ_G - is the density (compactness) of the material of the circuit board (Glass-Epoxy and Copper).

C_{Pa} - is thermal coefficient of the material of the circuit board (Glass-Epoxy and Copper).

From the equation it can be seen that the heat capacitance which is needed to solder a component having mass M and thermal coefficient C_p can be applied by increasing the layers area of the circuit board. The

increase of the area of the layer can be done in several ways. For example, adding layers, connecting between the layers in several locations and increasing the thickness of the layers.

The heat transfer operation from the second portion 4 to the first portion 3 will be described now with reference to FIG. 3, a cross section along line B-B of the circuit board.

The layers of the first portion 3 are connected to the layers of the second portion 4 by the plated via 18 and the plated verticaL face 20. The heat which stored within the second portion 4 is transferred from the second portion 4 to the first portion 3, as is shown by arrow 30. The heat melts the solder paste 24 around a leg 26 of the component 22 and solders the component 22 to the top substrate 2 at the leg top and leg bottom.

After the circuit board 1 passes the reflow oven the second portion 4 will be separated from the first portion 3. The separation between the two portion is done by breaking the frangible connection 32 between the first portion 3 to the second portion 4 as shown in FIG. 3. Furthermore, the breaking of the frangible connection 32 between the first portion 3 to the second portion 4 will cause disconnection of the layers 3 to 16 for proper operation of the circuit board 1.

Claims

1. A circuit board comprising:

at least one substrate having a first layer and at least a second layer wherein the first layer and at least the second layer are in use used for heating a component to be soldered to at least one of the layers.

2. A circuit board as claimed in claim 1 wherein the substrate has at least first and second portions which second portion being frangibly connected to the first portion.

3. A circuit board as claimed in claims 1 or 2 wherein there are provided a plurality of second layers.

4. A circuit board as claimed in claims 1,2 or 3 wherein at least one of the second layers is or are formed within the board.

5. A circuit board as claimed in claims 1,2,3 or 4 wherein the layers of the first portion are connected to the layers of the second portion wherein the first layer and at least one of the second layer are connected to each other.

6. A circuit board as claimed in claims 1,2,3,4 or 5 wherein the second portion is in use used as heat capacitor for accumulating a heat provided by a soldering device.

7. A circuit board as claimed in claim 6 wherein the soldering device is a reflow oven.

8. A circuit board as claimed in claims 1 to 7 wherein the heat transfers from the second portion to the first portion through the frangible connection.

9. A circuit board as claimed in any preceding claim wherein breaking of the frangible connection disconnects layers of the first portion from the layers of the second portion.

10. A circuit board as claimed in any preceding claim wherein the first layer and at least one second layer are made of copper.

11. A circuit board substantially as hereinbefore described with reference to and as illustrated by the drawing.

The Patent Office

Application No:	GB 9718570.6	**Examiner:**	Steven Davies
Claims searched:	1-11	**Date of search:**	22 January 1998

Patents Act 1977
Search Report under Section 17

Databases searched:

UK Patent Office collections, including GB, EP, WO & US patent specifications, in:

UK Cl (Ed.P): H1R-RAS, RAV

Int Cl (Ed.6): H05K-3/34

Other: Online database: WPI

Documents considered to be relevant:

Category	Identity of document and relevant passage	Relevant to claims
A	GB 2124035 A (S.T.C.)	

X	Document indicating lack of novelty or inventive step	A	Document indicating technological background and/or state of the art.
Y	Document indicating lack of inventive step if combined with one or more other documents of same category.	P	Document published on or after the declared priority date but before the filing date of this invention.
&	Member of the same patent family	E	Patent document published on or after, but with priority date earlier than, the filing date of this application.

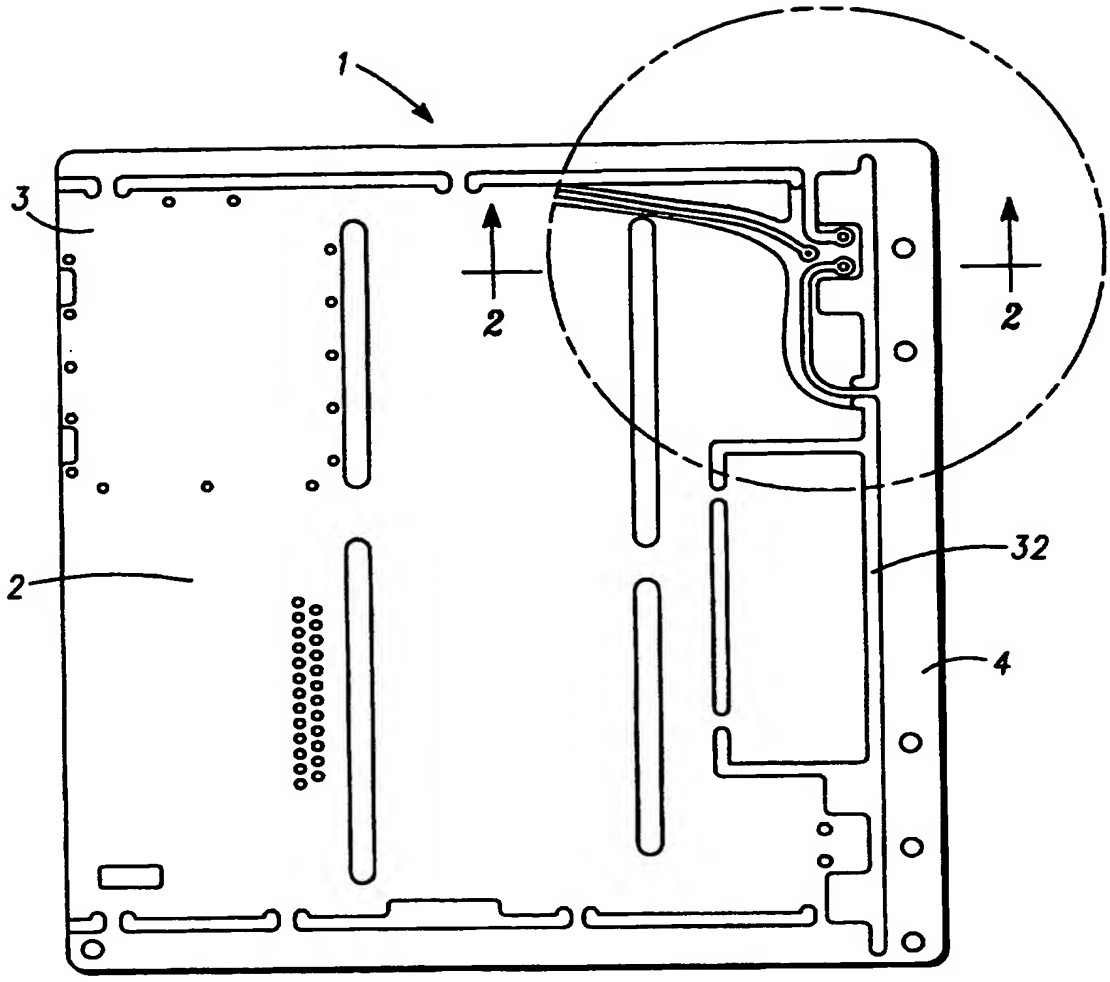

FIG. 1

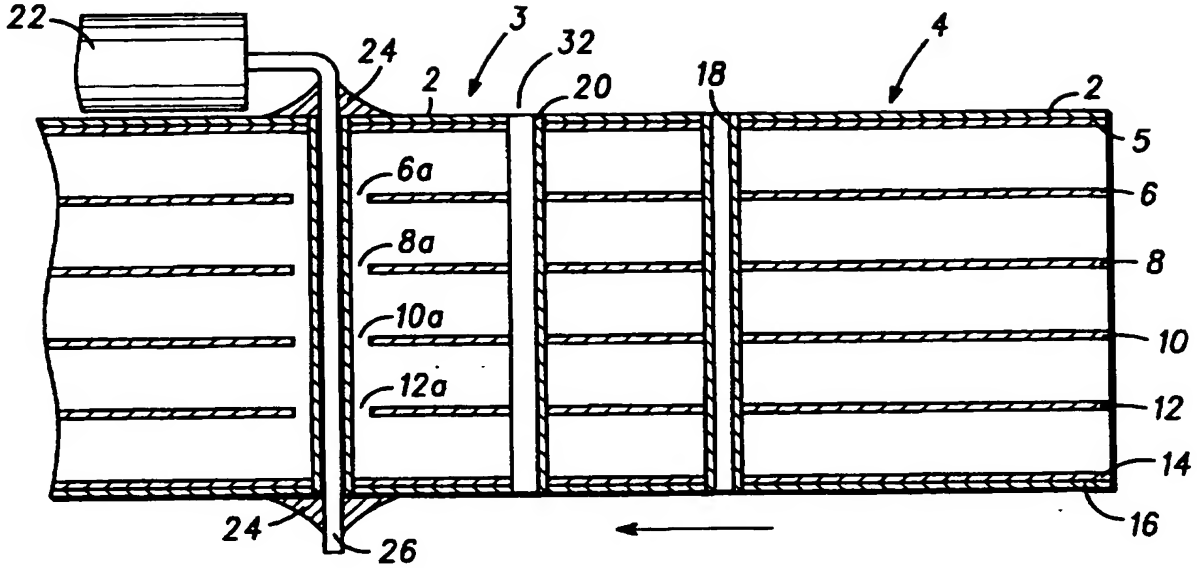

FIG. 2

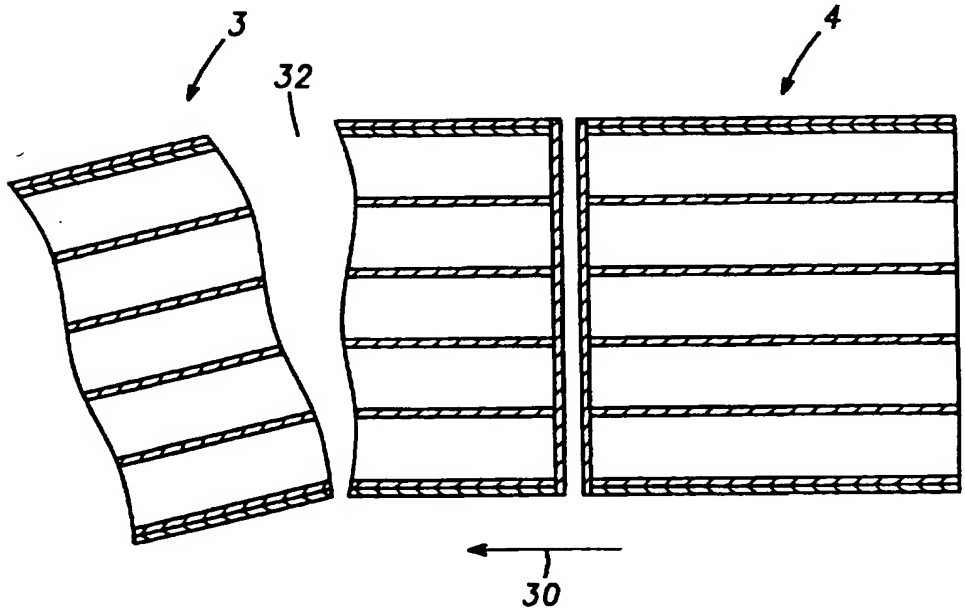

FIG. 3